A Low-IF RX Two-Point $\Sigma\Delta$-Modulation TX CMOS Single-Chip Bluetooth Solution

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***Abstract*—A new low-cost concept for a system-on-chip Bluetooth solution is proposed in this paper. The single chip includes all necessary baseband and RF parts to achieve full Bluetooth functionality and is implemented in a standard 0.25-μm CMOS technology. The two-point modulation $\Sigma\Delta$ fractional N phase-locked loop achieves a phase noise of −124 dBc/Hz at 3-MHz offset. The sensitivity of the embedded low-IF receiver is measured to be −82 dBm at a bit error rate of 0.1%. The power supply voltages for the digital and analog parts are internally regulated to 2.65 V. The maximum current consumption of the analog part is 60 mA.**

***Index Terms*—Communication systems, CMOS analog integrated circuits, CMOS digital integrated circuits, RF radio communication, RF receivers, RF transmitters, sigma–delta modulation, wireless LAN.**

I. Introduction

THE new short-range communication standard Bluetooth[1] wireless technologies enables the *ad hoc* networking of devices like mobile phones, laptops, palmtops, etc. in the unlicensed 2.4-GHz industrial–scientific–medical (ISM) band. Low cost, low power consumption, and small feature size are the main design issues for Bluetooth interfaces.

The used modern CMOS technology allows the integration of the baseband and RF parts on the same die, which minimizes cost and size. A careful floor planning, layout arrangements, isolation concept, system architecture, and circuit design are combined to achieve an optimum isolation between these parts and, thus, an optimized performance. Two completely independent and separately located voltage regulators minimize the digital crosstalk via the power supplies to the analog RF parts. A coil is implemented only for the voltage-controlled oscillator (VCO), whereas for the low-noise amplifier (LNA), an inductorless architecture is chosen. This prevents inductive crosstalk among transmit and receive path and reduces size. Closed-loop modulation and the earliest reasonable change into the digital domain in the receiver (RX) result in a robust crosstalk insensitive system solution. The single chip is highly integrated ($>1e6$ transistors) and realizes all system functions needed for communication under the Bluetooth standard. The single-chip system incorporates the transceiver for the 2.4-GHz ISM frequency band, with an on-chip output driver, a fully differential LNA, and a channel select filter. Together with the Bluetooth software "Pro-Blue," which includes the host controller interface (HCI) and link manager (LM), a system for Bluetooth wireless technology can be developed. To compose the complete hardware for a Bluetooth interface, only a few external (passive) components are needed. Thus, the main design issues for Bluetooth interfaces are attained with the proposed CMOS system on-chip Bluetooth solution.

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II. Architecture

The proposed low-cost single-chip architecture is depicted in Fig. 1. The baseband and RF parts will be discussed in detail below.

A. Baseband Part

The baseband part can be divided into the digital baseband section, the analog baseband section, and the link control section.

Within the digital baseband section, the demodulation unit is located, as well as the digital part of the $\Sigma\Delta$ fractional N phase-locked loop (PLL), and the control logic for the analog RF section, including timing, power, and Gaussian frequency shift keying (GFSK) modulation control for the PLL. An amplitude tunable Gaussian impulse forming filter is implemented to achieve the matching between the two modulation paths of the $\Sigma\Delta$ fractional N PLL.

In the analog baseband section, an 8-bit A/D converter for the radio signal strength indicator (RSSI) information from the RX is placed, as well as the 13-MHz crystal oscillator, its associated clock generation, and the voltage regulator for the digital power supply.

The link control section includes the link control management unit, and several I/O interfaces for application flexibility (e.g., four-wire pulse-code modulation (PCM) interface, universal asynchronous receiver transmitter (UART), I^2C interface, memory interface). During startup, the digital control reads the configuration information from the external E^2PROM, like

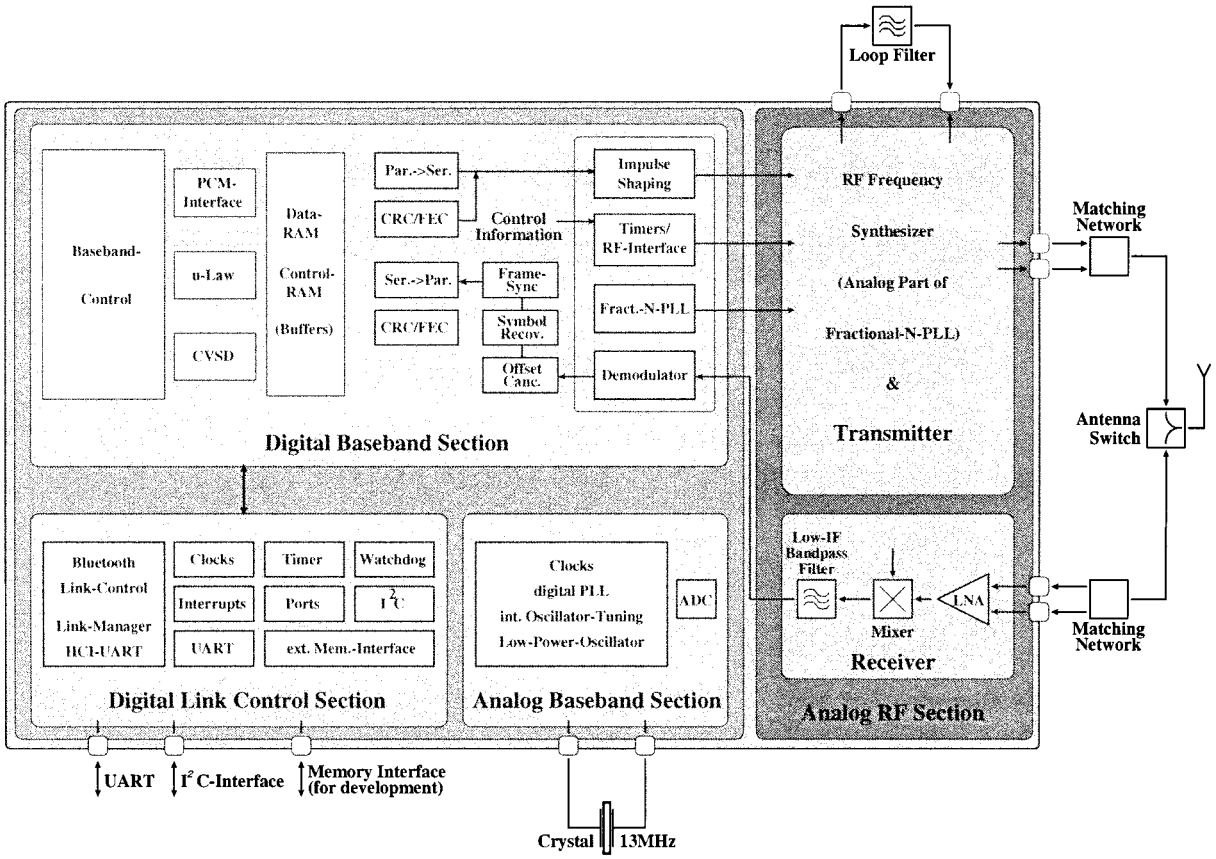

Fig. 1. Bluetooth SOC block diagram.

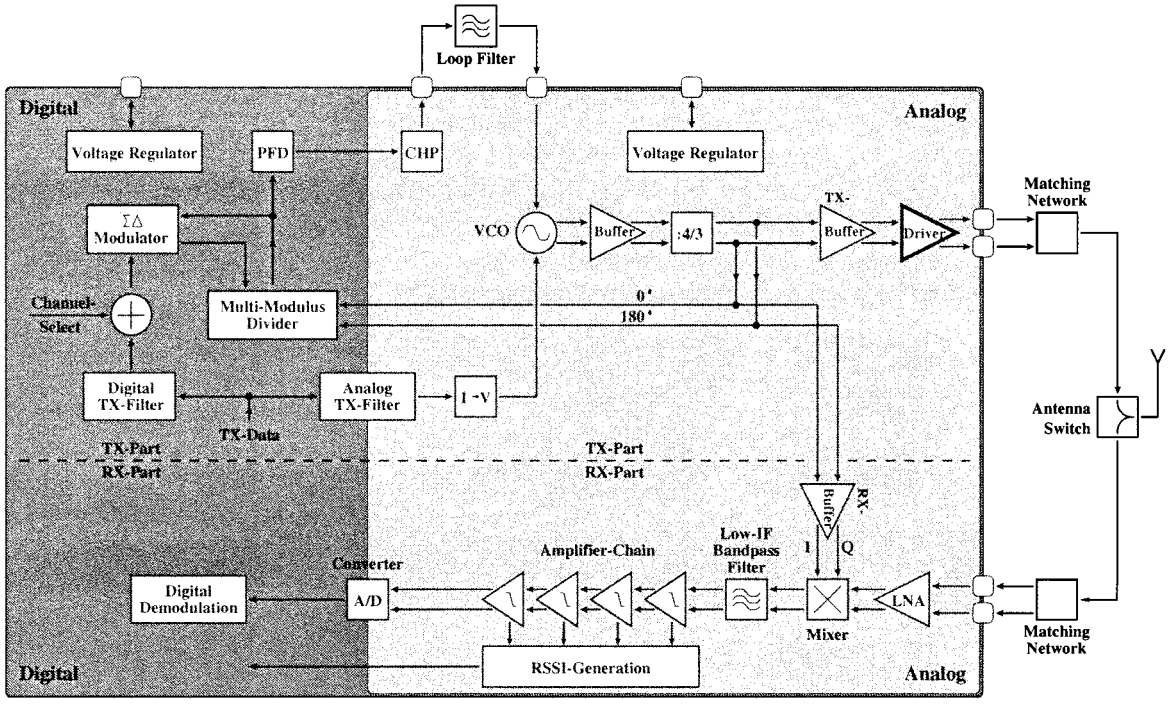

Fig. 2. Block diagram of the RF part.

crystal adjustment, the Bluetooth device address, etc. All other functions are done via host controller interface universal asynchronous receiver transmitter (HCI UART). Therefore, no hardware-specific firmware or software development has to be done.

B. RF Part

The RF section is depicted in more detail in Fig. 2. It can be divided into the transmitter (TX) and RX parts.

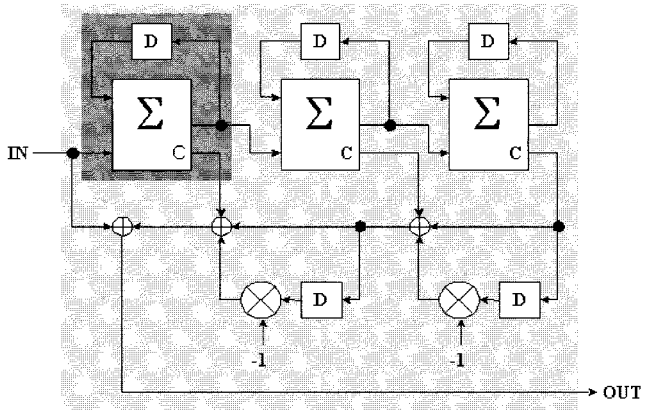

Fig. 3. Structure of the cascaded 1-1-1 MASH ΣΔ modulator.

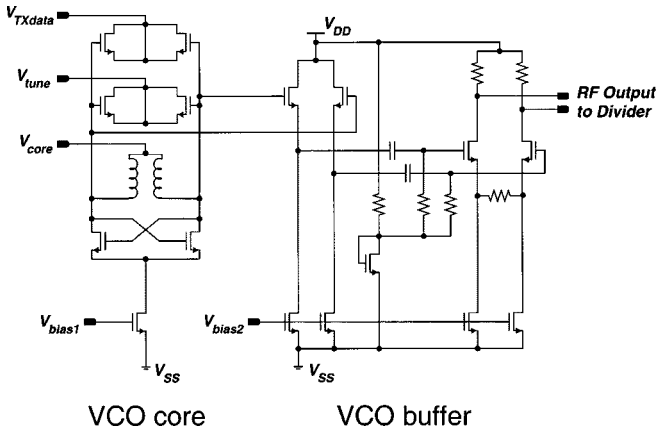

Fig. 4. Schematic of the 3.2-GHz VCO with additional modulation input.

1) TX Architecture: The part is based on the Bluetooth TX described in [2]. In the TX part, a ΣΔ fractional N PLL is realized. It contains a phase frequency detector (PFD), a chargepump (CHP), a multimodulus divider (MMD), a fully integrated VCO with a VCO buffer and 4/3 frequency converter, as well as a TX buffer and TX driver. The loop filter is realized as an external passive third-order filter. The maximum output power of the TXA driver is measured to be 0 dBm. The 13-MHz on-chip crystal oscillator provides the digital clock frequency and the reference for the phase-frequency detector.

Due to the feedback dynamics of the PLL, the maximum data rate is limited. To overcome the limited PLL bandwidth in order to achieve the 1-Mbit/s two-GFSK modulation, a two-point closed-loop modulation scheme is used. The gauss filtered data are injected into the loop at two different points via a low- and high-pass modulation path.

For the low-pass modulation, the digitally Gaussian shaped TX data are added to the channel word at the input of the ΣΔ modulator and, therefore, injected into the loop via the fully programmable MMD. Depending on the value of the parallel 7-bit output data stream of the ΣΔ modulator, the MMD divides the input frequency by a value of

$$N_{\mathrm{div}} = 128 + \sum_{n=0}^{6} b_n \cdot 2^n.$$

The structure of the cascaded multistage noise shaping (MASH) ΣΔ modulator is shown in Fig. 3. Its noise-shaping characteristic [3] allows the shift of low-frequency noise to higher frequencies, where it is attenuated by the loop filter.

The high-pass modulation is injected into the loop by direct VCO modulation. The incoming Gaussian shaped TX-impulse sequences are D/A converted within the analog section. The D/A conversion is done with weighted current sources. The output current is I/V converted and low-pass filtered next and given to the modulation input of the VCO.

The summation of both modulation paths allows to overcome the limited bandwidth of the PLL and, therefore, to modulate the VCO with frequencies beyond the loop bandwidth.

The fully integrated VCO is shown in Fig. 4. It contains a negative-transconductance (Gm) *LC* resonator with a cross-coupled pair of NMOS transistors as the active part. The *LC* resonator is implemented as an on-chip spiral inductor and NMOS varactors. These varactors are realized by using the depletion region of the capacitance characteristic of the transistors. By making use of these separate voltage-dependent capacitors within the VCO circuitry, the VCO frequency and, therewith, the transmit frequency, is finally Gaussian modulated—separately from the VCO tuning.

The VCO operates at 4/3 of the nominal TX frequency to avoid VCO pulling due to the output driver. The conversion to 2.4 GHz is achieved with an up-conversion image-reject mixer.

2) RX Architecture: The advantages of a "classical IF" RX and a zero-IF RX are combined in the chosen low-IF RX architecture [4]. Due to the possible integration of the channel-select filter, the integration level is equivalent with a zero-IF architecture, without the drawback of the well known dc-offset problem. Furthermore, the passive external high-Q filter for image rejection—needed in high-IF RXs—is replaced by a untuned, broadband, and, therefore, cheap filter. The IF of 1 MHz allows an ac coupling between the amplifier stages to remove static and dynamic offsets without affecting the desired signal. The RX is implemented fully differential to reduce the influence of switching noise from the digital circuits. Due to the low-crosstalk sensitivity, the LNA (Fig. 5) is implemented as an inductorless cascoded differential amplifier. A mixture of resistive and capacitive feedback is used to achieve a resistive input impedance. An external balun (matching network) is needed for the single-ended to differential conversion of the antenna signal.

The RF signal is down converted to the IF of 1 MHz by an in/quadrature phase (I/Q) mixer. A passive polyphase filter performs the 0° and 90° phase shift of the local oscillator (LO) signal for the receive mixer [5]. A fifth-order automatic adjusted polyphase filter is implemented for channel-select filtering in the complex domain. The complex signal processing allows the attenuation of the image without effecting the wanted signal at 1 MHz. As is well known from homodyne RXs and image reject mixers, a mismatch between the signal paths leads to a reduced image rejection [6]. The image frequency attenuation is directly correlated with the matching in the polyphase filter and LO mixers. The relative matching error between the resistors is kept smaller than 1%. The passband of the single-sideband bandpass is about 1 MHz, centered at 1 MHz. One-fourth of the filter area is occupied by switchable capacitors to tune out tolerances. The cutoff frequency can be adapted during the automatic

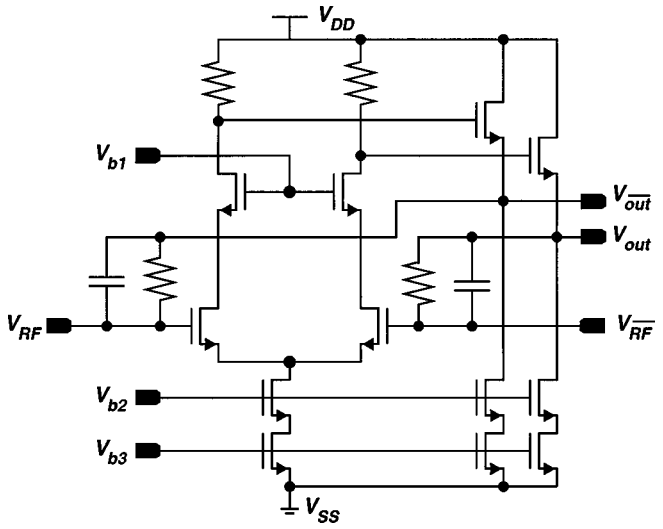

Fig. 5. Schematic of the inductorless LNA.

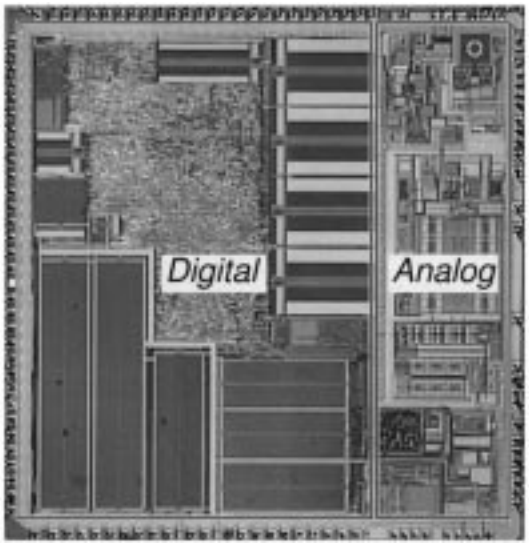

Fig. 6. Die photograph of the single chip.

adjustment before every receive time slot in the range of $\pm 20\%$. Two folded cascode operational amplifiers with a dc gain of 60 dB form a discrete pole of the filter. Each op-amp consumes 1.75 mW and contains an independent common-mode feedback loop. Overall, the filter has a linear input range of 600 mV, which is sufficient due to the output compression voltage of the front end. The noise figure of the filter is 22 dB. Due to the balanced design of the I/Q mixer, LO path, and polyphase filter, an overall RX image rejection of >28 dB is provided, which is sufficient for Bluetooth. The signals are amplified by a chain of ac-coupled amplifiers. The total gain of the amplifier chain is >80 dB. The analog representation of the RSSI signal is generated from the outputs of the first amplifiers and A/D converted for further digital processing. The dynamic range of the RSSI signal is >55 dB. A self-calibrating biasing is used in each amplifier stage to reduce static and dynamic offsets. The differential signal at the end of the amplifier chain is A/D converted and demodulated in the digital part.

Fig. 6 shows a chip photograph of the entire single chip. The baseband part covers roughly 3/4 and the RF part covers 1/4 of the occupied area. A careful floor planning and the use of guard rings and shieldings provide the optimum isolation between the analog and digital parts. In Fig. 7, the chip photograph of the RF part is shown. To give an idea of the required area of the introduced analog functional blocks, their placement is marked.

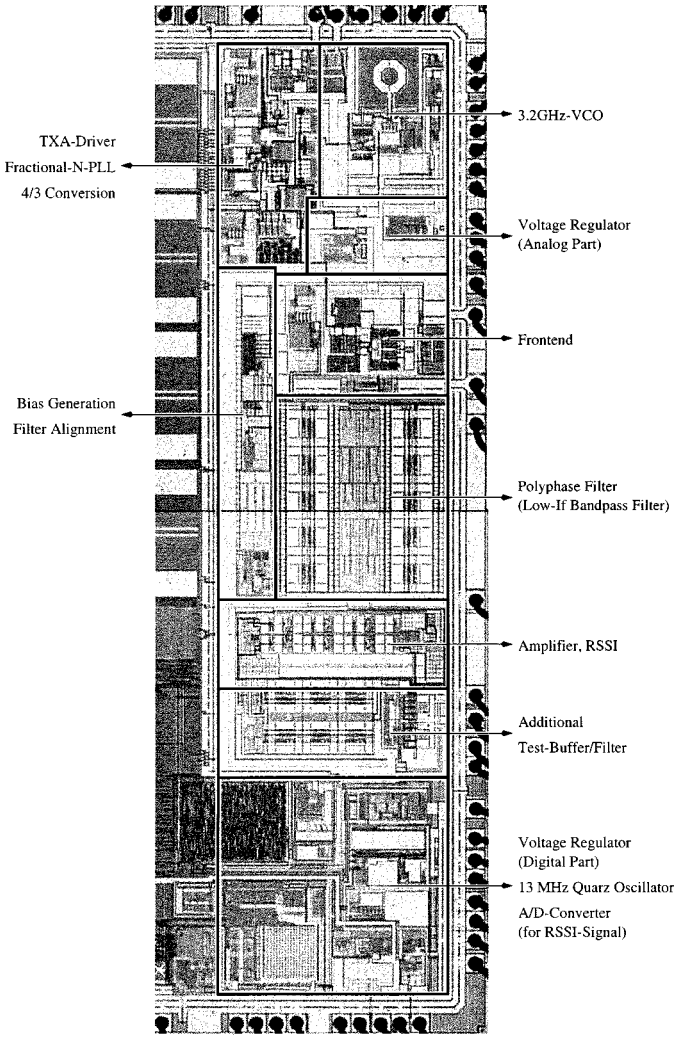

Fig. 7. Die photograph of the RF part.

III. Measurements

Initial measurement results indicate good function of all implemented analog and digital blocks. Successful bidirectional data transfers between the Bluetooth single chip and other listed Bluetooth transceivers over a distance of >14 m point out the functioning of the proposed concept.

The VCO provides a tuning sensitivity of about 635 MHz/V, by consuming 4 mA from the 2.65-V supply. The tuning range spans from 3.1 to 3.4 GHz. As shown in Fig. 8, the digitally controlled fractional N PLL locks at the 79 Bluetooth channels by achieving a channel independent phase noise of -124 dBc/Hz at 3-MHz offset.

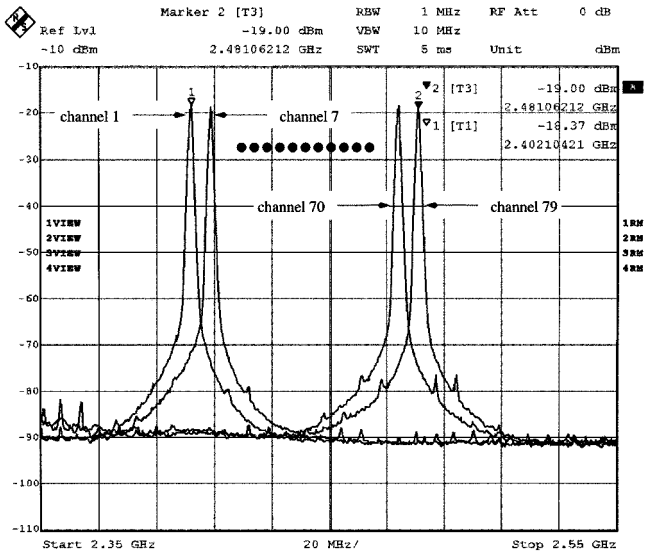

Fig. 8. Output spectrum of the PLL at different Bluetooth channels.

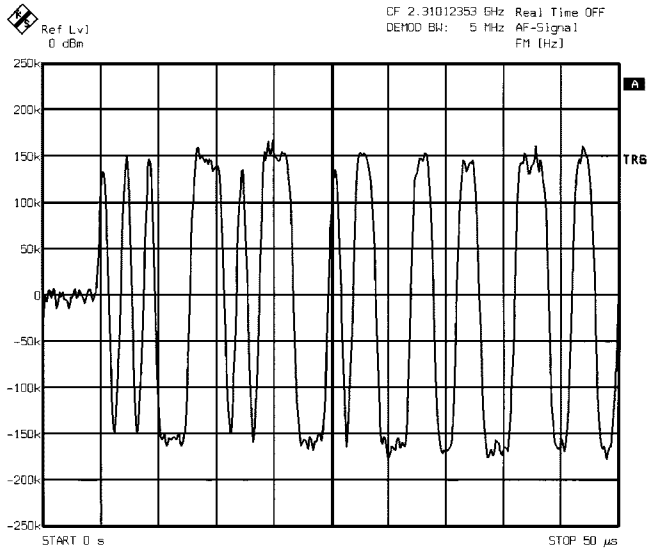

Fig. 9. Demodulated transmitted Gauss impulse sequence.

The Gaussian shape of the demodulated transmitted signal, shown in Fig. 9, indicates the wanted interaction of the two PLL modulation paths. The TXA driver provides an output power of 0 dBm. For higher power levels, an optional external power amplifier (PA) can be used.

The minimum detectable RX signal is −82 dBm at 0.1% BER, which is 12 dB better than required. The measured in-band blocker rejection is shown in Fig. 10. The minimum margin to the Bluetooth RX interference specification is 4 dB for the co-channel, which is set by the demodulator capture range. The adjacent channel rejection is set by the rolloff of the channel-select filter. The image rejection is 28–29 dB, which is nearly 10 dB better than required for the Bluetooth standard. In Fig. 11, the measured ac response of the fifth-order polyphase filter can be seen. After passing the automatic adjustment cycles, the ac response of the filter meets exactly the wanted characteristics. Furthermore, the available tuning range of the filter corner frequencies indicates that fabrication tolerances can easily be balanced.

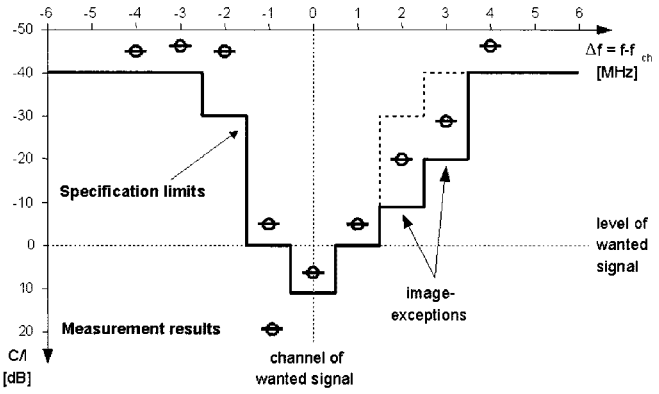

Fig. 10. RX interference performance at 0.1% BER.

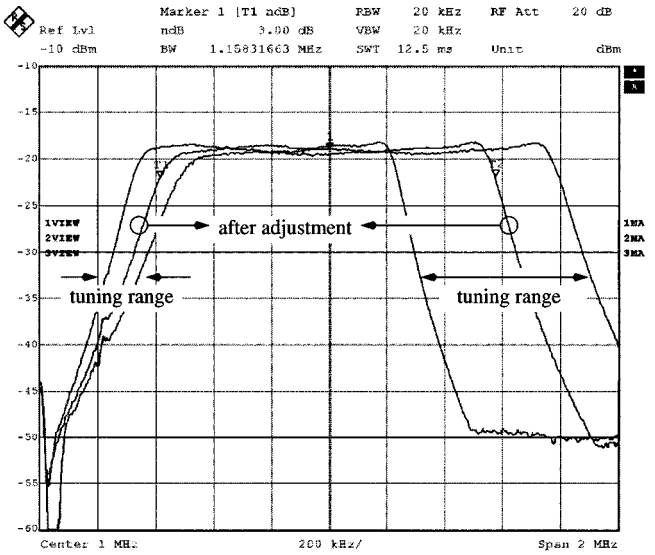

Fig. 11. AC response of the fifth-order polyphase filter.

The maximum current consumption of the analog part is 60 mA. The benefit of an inductorless RX is the low-crosstalk sensitivity and the small size, which simplifies a Bluetooth single-chip solution. The supply voltage of the digital and analog parts is 2.65 V, and both are internally regulated.

IV. Conclusion

A low-cost concept for a CMOS system on chip Bluetooth solution has been presented in this paper. The measurement results meet the Bluetooth specifications[2] and show the suitability of the presented single-chip concept.

The crosstalk between the analog and digital parts is the drawback of single-chip solutions. This effect is kept small by the proposed crosstalk-insensitive system concept, circuit design, and layout. In a further redesign, the current consumption of the baseband and RF parts will be reduced and the RX sensitivity increased. Due to the need of only a few external elements and a reasonable power consumption, the proposed single-chip solution fulfills the main design issues for small-size low-cost Blue-

[2]Bluetooth Version 1.0B, 1999. [Online]. Available: http://www.bluetooth.com

tooth interfaces. Within the next redesign step, full Bluetooth performance and reduced power consumption will be achieved.

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REFERENCES

[1] J. P. K. Gilb, "Bluetooth radio architectures," in *IEEE RFIC Symp. Dig.*, June 2000, pp. 3–6.
[2] D. Theil, C. Dürdodt, A. Hanke, S. Heinen, S. vanWaasen, D. Seippel, D. Pham-Stäbner, and K. Schumacher, "A fully integrated CMOS frequency synthesizer for Bluetooth," in *IEEE RFIC Symp. Dig.*, May 2001, pp. 103–106.
[3] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta–Sigma Data Converters: Theory, Design, and Simulation*. Piscataway, NJ: IEEE Press, 1997.
[4] J. Crols and M. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1483–1492, Dec. 1995.
[5] J. Janssens, M. Steyaert, B. De Muer, M. Borremans, and N. Itoh, "A 2 V CMOS cellular transceiver front-end," in *IEEE Int. SSC Conf.*, 2000, pp. 142–143.
[6] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399–1409, Dec. 1995.

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